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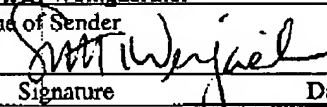
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MAY 23 2006

1103179-0009

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Edward Colles Nevill
Serial No. : 10/066,475
Filed : February 1, 2002
For : INTEROPERABILITY WITH MULTIPLE
INSTRUCTION SETS
Examiner : Kenneth R. Coulter
Group Art Unit : 2141

CERTIFICATE OF TRANSMISSION UNDER 37 C.F.R. 1.8	
I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on the date indicated below at the facsimile number 571-273-8300.	
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Kenneth R. Coulter
Group 2141
Commissioner of Patents
U.S. Patent and Trademark Office
Washington, D.C. 20231

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PROPOSED AGENDA FOR SCHEDULED TELEPHONE DISCUSSION
(For Purposes Of Discussion Only)

Dear Examiner Coulter:

Solely to facilitate our discussion, we provide you with a proposed agenda for our
telephone conference this Thursday May 25, 2006.

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1. Request For Clarification In View Of Prior Prosecution History

We would like to address the outstanding rejection mailed on February 15, 2006, in which all pending claims were rejected over U.S. Patent No. 5,115,500 to Larsen ("Larsen"). Larsen corresponds to European Publication No. 324,308, a reference that Applicant disclosed to the U.S. Patent and Trademark Office (USPTO) in the prosecution of: (i) the application, Serial No. 09/840,557 ("the '577 Application"), which issued as original patent; and the parent of the '577 Application, Serial No. 08/477,781 ("the '781 Application"). See '577 Application, Paper No. 3 (Information Disclosure Statement received on October 13, 1998) and '781 Application, Paper Nos. 5, and 8 (Information Disclosure Statement received on August 21, 1995 and Response and Amendment, received on April 14, 1997, respectively).

During the prosecution which ultimately led to the original patent, no claims were ever rejected over Larsen or its European counterpart in either of the '577 or '781 Applications. Nevertheless, out of an abundance of caution, Applicant distinguished the then pending claims over Larsen in prosecuting the '781 Application:

Applicant submits that this [claimed invention] is novel over Larsen, where three most significant bits of the program counter differentiate between memory areas containing different instructions sets. For example, a significant drawback of the arrangement shown in the Larsen document is that the memory address space must be partitioned into pre-defined memory areas corresponding to the respective instruction sets. This can be seen on Figure 2 of Larsen, and in the abstract which states that "[i]nstructions in different formats which are normally compatible are placed in *pre-defined* or segregated areas of the instruction store (2)... Decoding is then determined in part by where in the instruction store the instruction resided when fetched, and the specific instruction itself." (emphasis added).

The arrangement in Larsen places constraints on the designer of a system using such a microprocessor. The memory address space is physically partitioned, so that predetermined memory areas are available for each of the instruction sets. This takes no regard of the actual needs of a particular piece of software, where the amount of memory needed in each of the instruction sets will depend on the way in which the software is written. On the contrary, whether or not the software designer wishes to use "machine type 2" instructions, in the Larsen system the high order one-eighth of the instruction store 2 will have to be provided in the physical memory in case the software

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designer *might* wish to use machine type 2 instructions. A converse argument applies to the lower seven-eighths of the instruction store which may or may not be required, but which have to be provided in case they are required.

In short, Larsen provides a system which allows two normally incompatible instruction sets to be executed with in a single microprocessor, but which is by its very nature inflexible in that it required *predetermined* portioning of the memory page.

This is not just a trivial difference. On the contrary, it avoids the need for the partitioning of memory space as required by Larsen. It allows the entire memory area to be partitioned by the *software designer* rather than by the *hardware designer* - an important feature for general purpose microprocessors of the type described in the present application and in Larsen. Thus, the software designer is free to choose how much of the memory space is to be used for the instruction set; and that allocation can be easily and dynamically changed when another software program is loaded. The arrangement also allows the freedom to interleave instructions of the various instruction sets, which is denied to the user of the Larsen device.

See Serial No. 08/447,781, Paper No. 8 at 14-15 (emphasis in original).

The patentable distinction of claims of the original patent, in fact, has been formally recognized. Allowance of claims of the original patent -- now pending in this reissue application -- was accompanied by a Statement of Reasons for Allowance that explicitly acknowledged the distinction of the then pending claims over the art of record, which included the European counterpart to the Larsen reference. See Serial No. 08/847,557, Paper No. 6 at 2.

In view of the role of Larsen in the prosecution history leading to the pending claims, Applicant respectfully requests an opportunity to discuss, and gain a better understanding of, the basis for the pending rejections.

2. Discussion of Claims Added During Reissue

As with the issued claims of the original patent, Applicant believes that among other possible distinctions, the pending reissue claims all contain one or more limitations that are not disclosed or suggested by, and would not be possible based upon, Larsen's description of a

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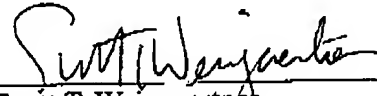
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partitioned memory where the address of the instruction also designates the format of the instruction.

Applicant thanks the Examiner for his attention to this request and, in advance, for his time during the scheduled teleconference. If any questions arise, the Examiner is requested to contact Applicant's representative.

Dated: May 23, 2006

Respectfully submitted,



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